THE CLAIMS

1. (Currently Amended) A semiconductor memory device comprising:

a sense amplifier group configured in a hierarchy to read out data from a memory cell;

a complementary signal line group for connecting a sense amplifier of a lower hierarchy level of said sense amplifier group with a sense amplifier of a higher hierarchy level of said sense amplifier group and connecting the sense amplifier of the lower hierarchy level of said sense amplifier group with said memory cell; and

a control circuit suppressing a drive of complementary signal lines of said complementary signal line group by the sense amplifier of [a] lower hierarchy level [connected to said complementary signal lines], and rendering active the sense amplifier of [a] higher hierarchy level [connected to said complementary signal lines,] before a potential difference between said complementary signal lines reaches a level of power supply voltage;

wherein, when a sense amplifier of higher hierarchy level of said sense amplifier group is active, said active sense amplifier has no electrical interconnection with the complementary signal lines of said complementary signal line group for connecting said active sense amplifier with the sense amplifier of lower hierarchy level of said sense amplifier group or said memory cell.

2. (Currently Amended) The semiconductor memory device according to claim 1, further comprising a write driver group configured in a hierarchy to write data into a memory cell, wherein

a write driver of a lower hierarchy level of said write driver group and a write driver of a higher hierarchy level of said write driver group are connected to each other by said complementary signal lines and a write designation signal line,

said write driver of [a] higher hierarchy level outputs write data and inverted data thereof to said complementary signal lines [of a lower hierarchy level connected to said write driver of a higher hierarchy level,] and drives the write designation signal line [of a lower hierarchy level connected to said write driver of a higher hierarchy level] at a predetermined logic value, and

said write driver of [a] lower hierarchy level is rendered active when a [the]write designation signal output on the write designation line [of a] by the write driver of higher hierarchy level [connected to said write driver of a lower hierarchy level] attains said predetermined logic value.

3. (Currently Amended) The semiconductor memory device according to claim 1, further comprising a write driver group configured in a hierarchy to write data into a memory cell, wherein

a write driver of a lower hierarchy level of said write driver group and a write driver of a higher hierarchy level of said write driver group are connected to each other by said complementary signal lines,

said write driver of a higher hierarchy level outputs write data to one signal line of said complementary signal lines [of a lower hierarchy level connected to said write driver of a higher hierarchy level,] and drives [the other] another signal line of said complementary signal lines [of a lower hierarchy level] at a predetermined potential in a range other than the range of change of said other signal line in a read mode, and

said write driver of a lower hierarchy level is rendered active when said [other] another signal line attains said predetermined potential.

4. (Currently Amended) The semiconductor memory device according to claim 3, wherein

said write driver of a lower hierarchy level comprises a logical element connected to said [other] another signal line,

said logical element providing an output of a first logic value when the potential of said [other] another signal line is in the range of change in a read mode and provides an output of a second logic value when the potential of said [other] another signal line is in a range other than said range.

5. (Currently Amended) The semiconductor memory device according to claim 1, wherein a [predetermined] a lower hierarchy sense amplifier in said sense amplifier group includes

a transmission gate provided between complementary signal lines for connecting the lower hierarchy sense amplifier with a sense amplifier of a higher hierarchy level [and complementary signal lines of a lower hierarchy level],

said transmission gate being rendered conductive when in a data write mode.

6. (Original) The semiconductor memory device according to claim 1, wherein a predetermined sense amplifier in said sense amplifier group includes

a circuit to fetch a potential of complementary signal lines of a higher hierarchy level connected to said predetermined sense amplifier, and

an N channel MOS transistor provided between said circuit and complementary signal lines of a lower hierarchy level connected to said predetermined sense amplifier,

said N channel MOS transistor being rendered conductive when in a data write mode.

7. (Currently Amended) The semiconductor memory device according to claim 1, wherein [predetermined] a pair of complementary signal lines of said complementary signal line group are driven at an amplitude smaller than the amplitude of power supply voltage in a data write mode,

wherein [a] said sense amplifier of a lower hierarchy level connected to said [predetermined] said pair of complementary signal lines, includes

an amplify circuit amplifying potentials of said [predetermined] pair of complementary signal lines, and

a P channel MOS transistor provided between said amplify circuit and said [predetermined] pair of complementary signal lines,

wherein, in a data write mode, said P channel MOS transistor is rendered conductive to have potentials of said [predetermined] pair of complementary signal lines applied to said amplify circuit, and after said application, said P channel MOS transistor is rendered conductive, and said amplify circuit amplifies said applied potentials at a logic amplitude of power supply voltage, and another pair of complementary signal lines of a lower hierarchy level connected to said sense amplifier of a lower hierarchy level [connected to said predetermined complementary signal lines] are driven based on said amplified potentials.

8. (Currently Amended) The semiconductor memory device according to claim 1, wherein [a predetermined] said lower hierarchy sense amplifier [in said sense amplifier group] includes

an amplify circuit connected to complementary signal lines [of a lower hierarchy level] connecting to said memory cell, and

a latch circuit connected to said amplify circuit and connected to complementary signal lines [of a] connecting to the higher hierarchy level sense amplifier,

wherein said amplify circuit fetches potentials of said complementary signal lines connecting to said memory cell [of a lower hierarchy level] at a timing based on a first clock to amplify said fetched potentials, and provide said amplified potentials to said latch circuit,

wherein said latch circuit drives said complementary signal lines [of a] connecting to the higher hierarchy level sense amplifier at latched said amplified potentials at a timing based on a second clock different from said first clock.

9. (Currently Amended) The semiconductor memory device according to claim 8, wherein said complementary signal lines [of a] connecting to the higher hierarchy level [connected to said predetermined] sense amplifier are precharged at a timing based on said second clock, and

[a sense amplifier of a] said higher hierarchy level sense amplifier [than said predetermined sense amplifier] is rendered active at a timing based on said second clock.